wherein said central hardware device communicates requests from said first node to said second node but not to said other node.

REMARKS

This Preliminary Amendment is made to update the Specification's "Cross-Reference to Related Applications" with the application numbers and filing dates of the applications listed therein.

This amendment also corrects a typographical error in claim 1. As originally filed, claim 1 inadvertently omitted the word "not" before the concluding phrase "to said other node." That omission is corrected by this amendment. No new matter is added, because the Summary of the Invention as originally filed correctly stated that, "The central hardware device transmits requests from the said requesting node to the said target node but <u>not</u> to any other node." (emphasis added)

Applicants submit that this application is now in condition for examination, and respectfully request early and favorable consideration of its claims. The Examiner is urged to call the undersigned at the below-listed telephone number if, in the Examiner's opinion, such a phone conference would expedite or aid in the search or examination of this application.

Respectfully submitted,

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ATTACHMENT A TO AMENDMENT

Marked-up Version Showing Changes Made by this Amendment

Changes made by this amendment are marked-up below, showing [deletions in brackets] and insertions underlined .

In the Specification

Page 1, line 8, through page 2, line 9, has been amended as follows.

U.S. patent application serial number [__/___,___] 10/045,798 by T. B. Berg et al. (BEA919990003US1) entitled "Method And Apparatus For Increasing Requestor Throughput By Using Data Available Withholding" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,927 by T. B. Berg et al. (BEA920000017US1) entitled "Method And Apparatus For Using Global Snooping To Provide Cache Coherence To Distributed Computer Nodes In A Single Coherent System" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,821 by T. B. Berg et al. (BEA920000018US1) entitled "Multi-level Classification Method For Transaction Address Conflicts For Ensuring Efficient Ordering In A Two-level Snoopy Cache Architecture" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,564 by S.G. Lloyd et al. (BEA920000019US1) entitled "Transaction Redirection Mechanism For Handling Late Specification Changes And Design Errors" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,797 by T. B. Berg et al. (BEA920000020US1) entitled "Method And Apparatus For Multi-path Data Storage And Retrieval" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,925 by T. B. Berg et al. (BEA920000022US1) entitled "Distributed Allocation Of System Hardware Resources For Multiprocessor Systems" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,926 by W. A. Downer et al. (BEA920010030US1) entitled "Masterless Building Block Binding To Partitions" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,774 by W. A. Downer et al. (BEA920010031US1) entitled "Building Block Removal From Partitions" was filed on [January __, 2002] January 9, 2002.

U.S. patent application serial number [__/___,___] 10/045,796 by W. A. Downer et al. (BEA920010041US1) entitled "Masterless Building Block Binding To Partitions Using Identifiers And Indicators" was filed on [January __, 2002] January 9, 2002.

In the Claims

Claim 1 has been amended as follows.

1. (Amended) A multiprocessor computer system comprising:

first, second and other processing nodes, each including at least one processor;

a communication pathway connecting said nodes and including a central hardware device;

a shared, distributed system memory, a portion of said shared system memory being coupled to said processors and to said communication pathway; and

wherein said central hardware device communicates requests from said first node to said second node but not to said other node.

The transmission ends with this page